FIG. 1

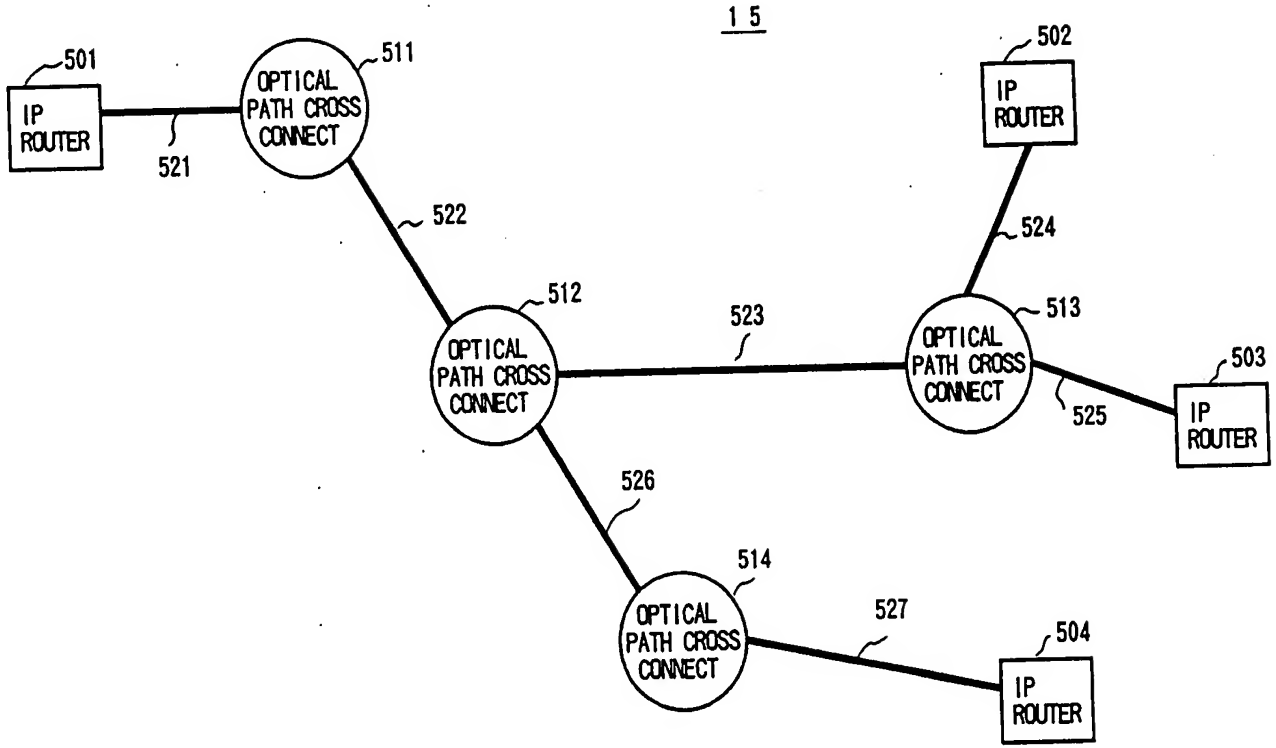
15
501
IP ROUTER
521
511
OPTICAL PATH CROSS CONNECT
522
512
OPTICAL PATH CROSS CONNECT
523
526
514
OPTICAL PATH CROSS CONNECT
527
504
IP ROUTER
502
IP ROUTER
524
513
OPTICAL PATH CROSS CONNECT
525
503
IP ROUTER

FIG. 2

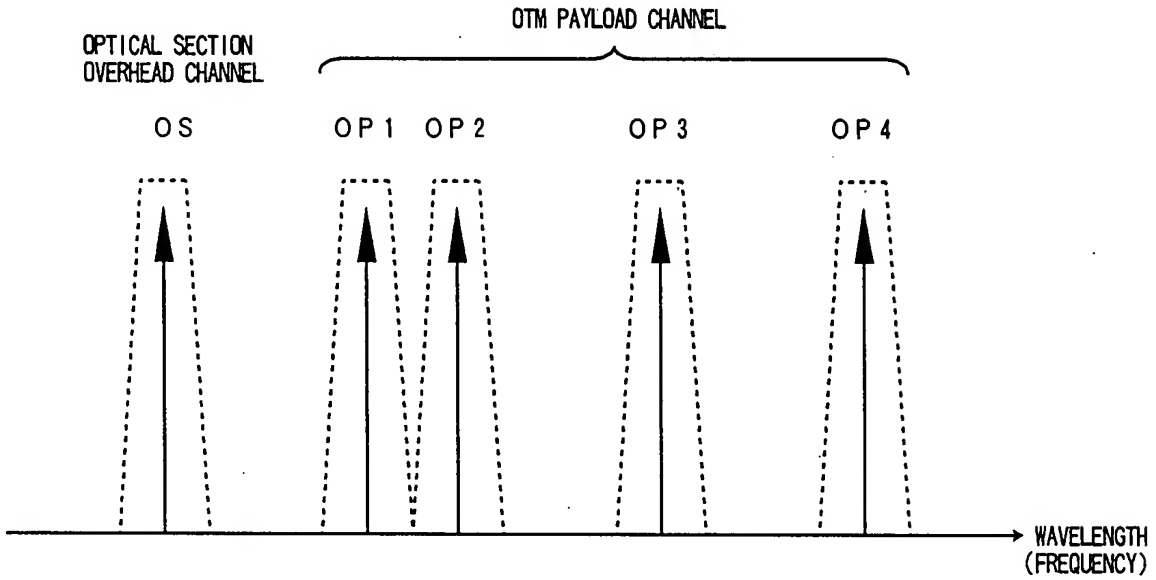
OTM PAYLOAD CHANNEL
OPTICAL SECTION
OVERHEAD CHANNEL
OS
OP1
OP2
OP3
OP4
WAVELENGTH
(FREQUENCY)

FIG. 3

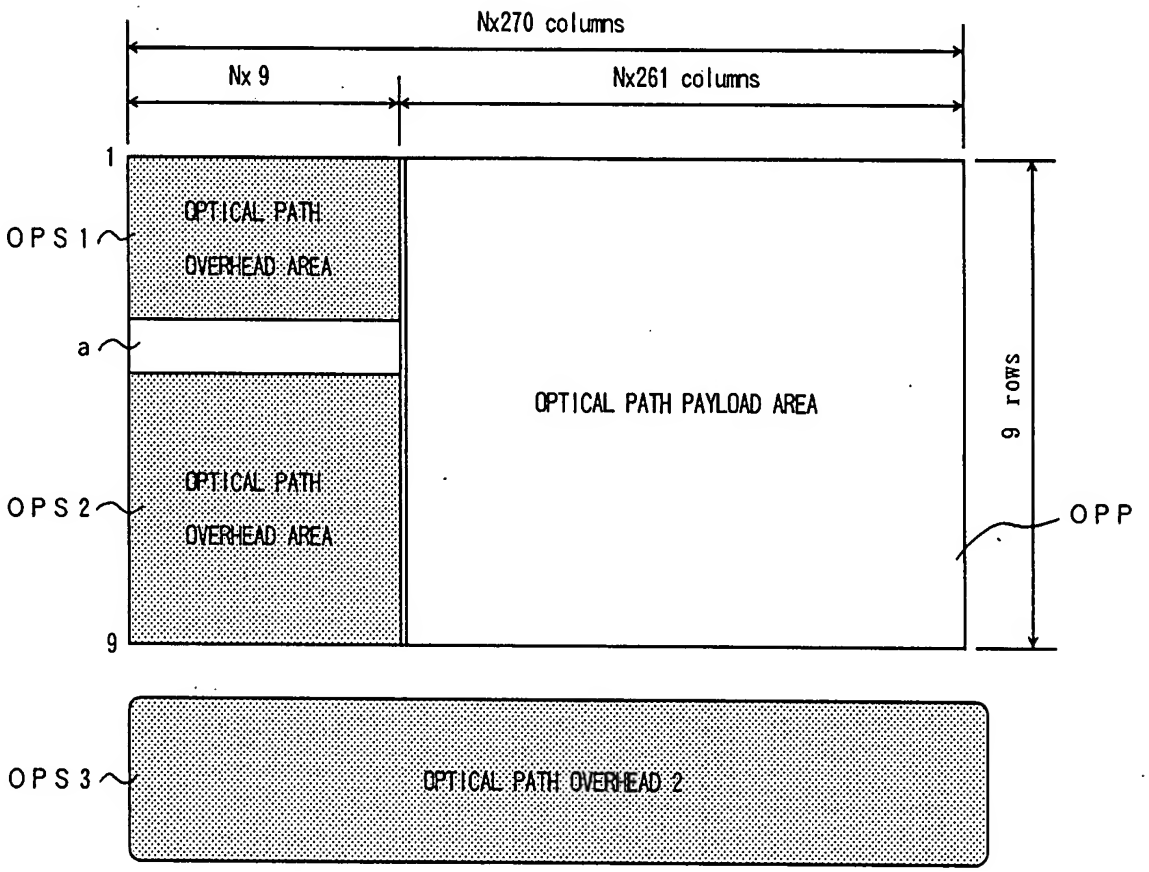
Nx270 columns
Nx 9
Nx261 columns
1
OPS 1
OPTICAL PATH
OVERHEAD AREA
a
OPS 2
OPTICAL PATH
OVERHEAD AREA
9
OPTICAL PATH PAYLOAD AREA
9 rows
OPP
OPS 3
OPTICAL PATH OVERHEAD 2

FIG. 4

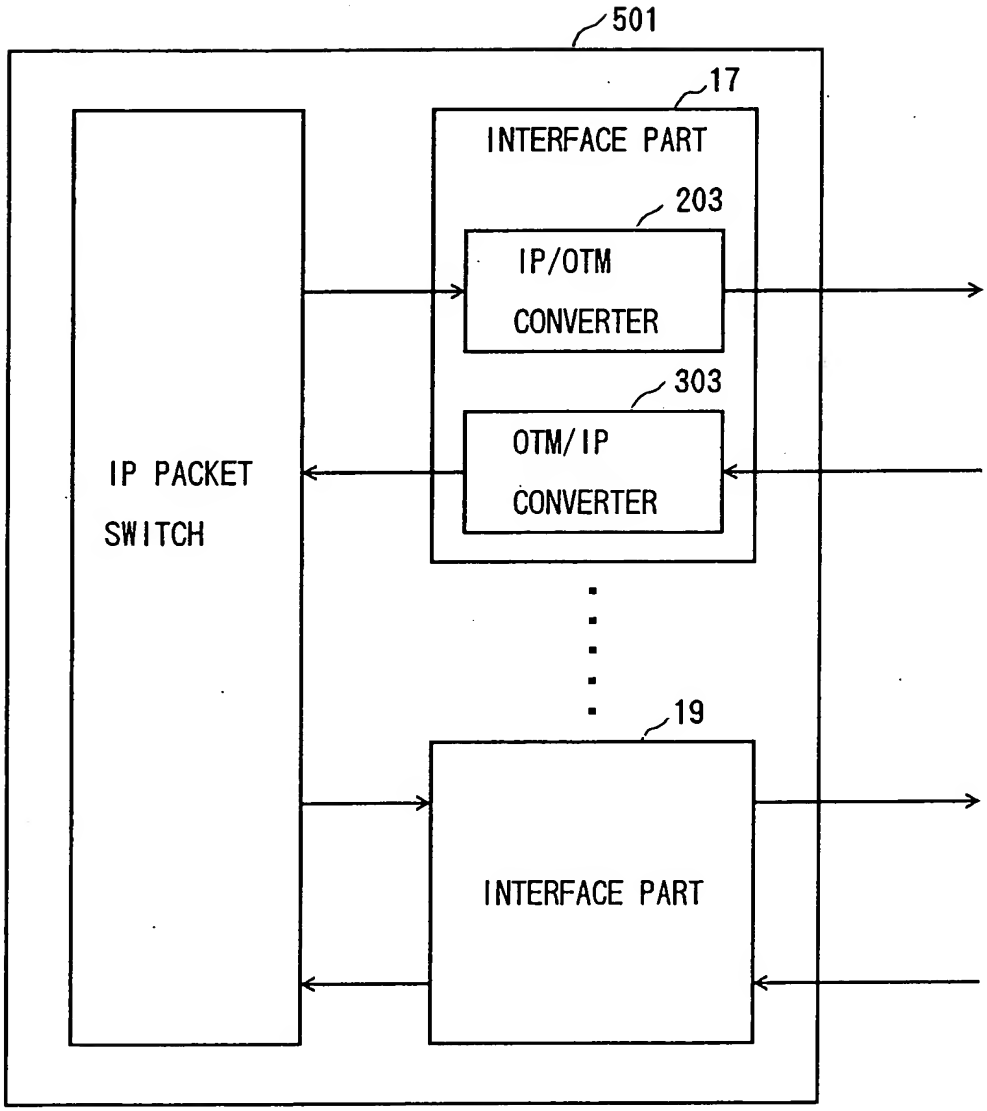
501
17
INTERFACE PART
203
IP/OTM
CONVERTER
303
OTM/IP
CONVERTER
IP PACKET
SWITCH
19
INTERFACE PART

FIG. 5

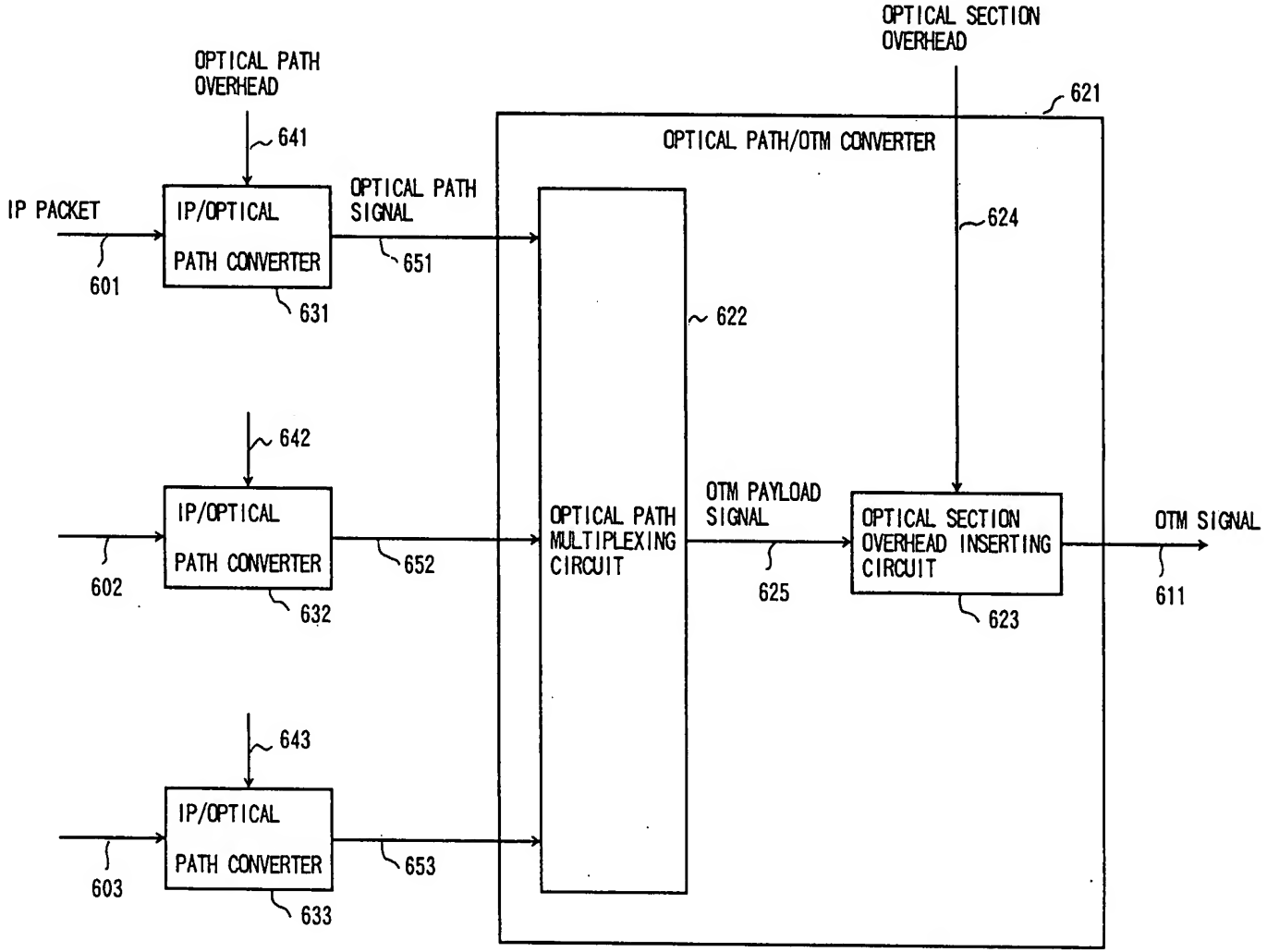
OPTICAL SECTION OVERHEAD
OPTICAL PATH OVERHEAD
641
621
OPTICAL PATH/OTM CONVERTER
IP PACKET
IP/OPTICAL PATH CONVERTER
OPTICAL PATH SIGNAL
624
601
651
631
622
642
IP/OPTICAL PATH CONVERTER
OPTICAL PATH MULTIPLEXING CIRCUIT
OTM PAYLOAD SIGNAL
OPTICAL SECTION OVERHEAD INSERTING CIRCUIT
OTM SIGNAL
602
652
632
625
623
611
643
IP/OPTICAL PATH CONVERTER
603
653
633

FIG. 6

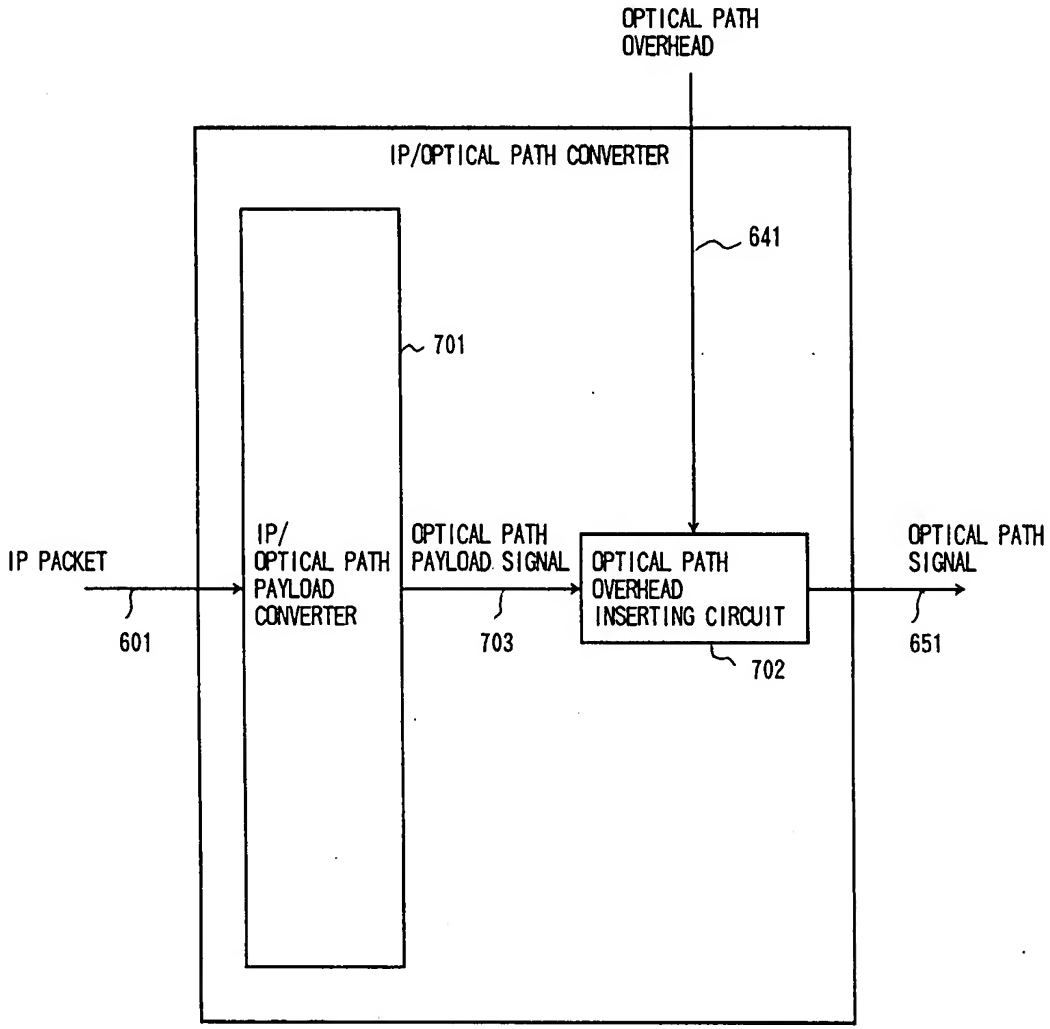
OPTICAL PATH
OVERHEAD
IP/OPTICAL PATH CONVERTER
641
701
IP PACKET
601
IP/
OPTICAL PATH
PAYLOAD
CONVERTER
OPTICAL PATH
PAYLOAD SIGNAL
703
OPTICAL PATH
OVERHEAD
INSERTING CIRCUIT
702
OPTICAL PATH
SIGNAL
651

FIG. 7

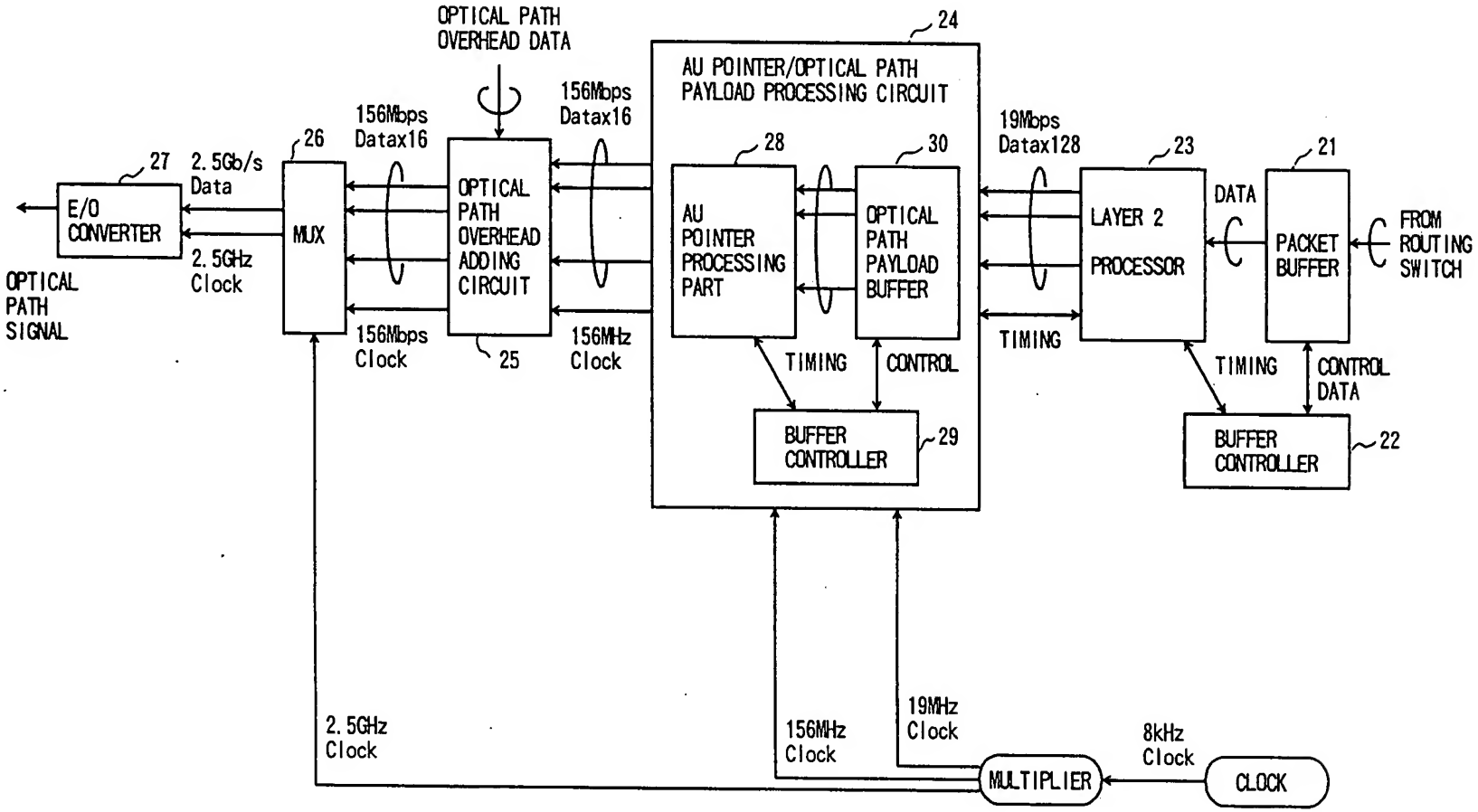
OPTICAL PATH
OVERHEAD DATA
24
AU POINTER/OPTICAL PATH
PAYLOAD PROCESSING CIRCUIT
156Mbps
Datax16
156Mbps
Datax16
19Mbps
Datax128
28
30
23
21
27
2.5Gb/s
Data
26
E/O
CONVERTER
MUX
OPTICAL
PATH
OVERHEAD
ADDING
CIRCUIT
AU
POINTER
PROCESSING
PART
OPTICAL
PATH
PAYLOAD
BUFFER
LAYER 2
PROCESSOR
DATA
PACKET
BUFFER
FROM
ROUTING
SWITCH
OPTICAL
PATH
SIGNAL
2.5GHz
Clock
156Mbps
Clock
25
156MHz
Clock
TIMING
CONTROL
TIMING
TIMING
CONTROL
DATA
BUFFER
CONTROLLER
29
BUFFER
CONTROLLER
22
2.5GHz
Clock
156MHz
Clock
19MHz
Clock
8kHz
Clock
MULTIPLIER
CLOCK

FIG. 8

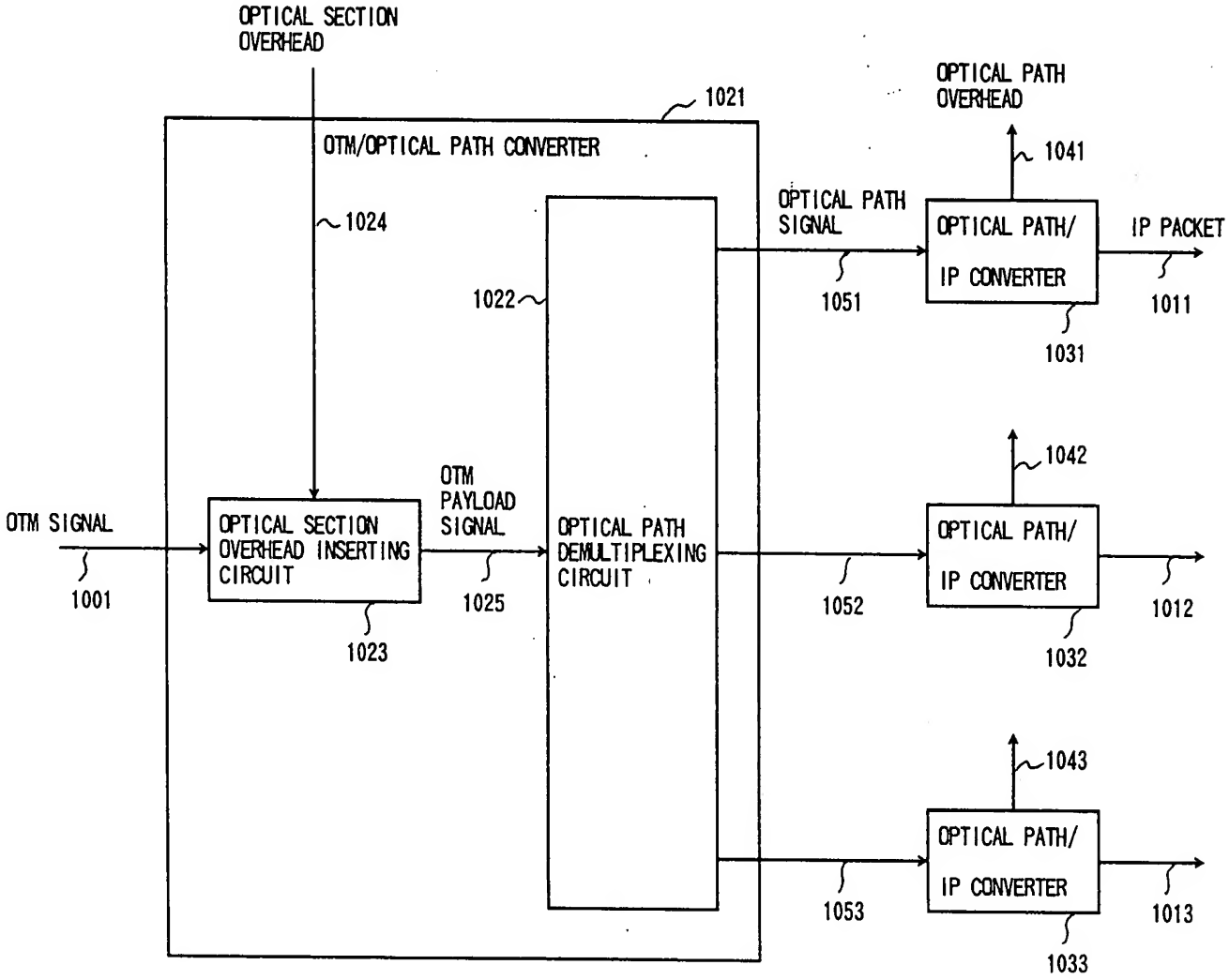
OPTICAL SECTION OVERHEAD
1021
OTM/OPTICAL PATH CONVERTER
OPTICAL PATH OVERHEAD
1041
1024
OPTICAL PATH SIGNAL
OPTICAL PATH/ IP CONVERTER
IP PACKET
1022
1051
1011
1031
1042
OTM PAYLOAD SIGNAL
OTM SIGNAL
OPTICAL SECTION OVERHEAD INSERTING CIRCUIT
OPTICAL PATH DEMULTIPLEXING CIRCUIT
OPTICAL PATH/ IP CONVERTER
1001
1025
1052
1012
1023
1032
1043
OPTICAL PATH/ IP CONVERTER
1053
1013
1033

FIG. 9

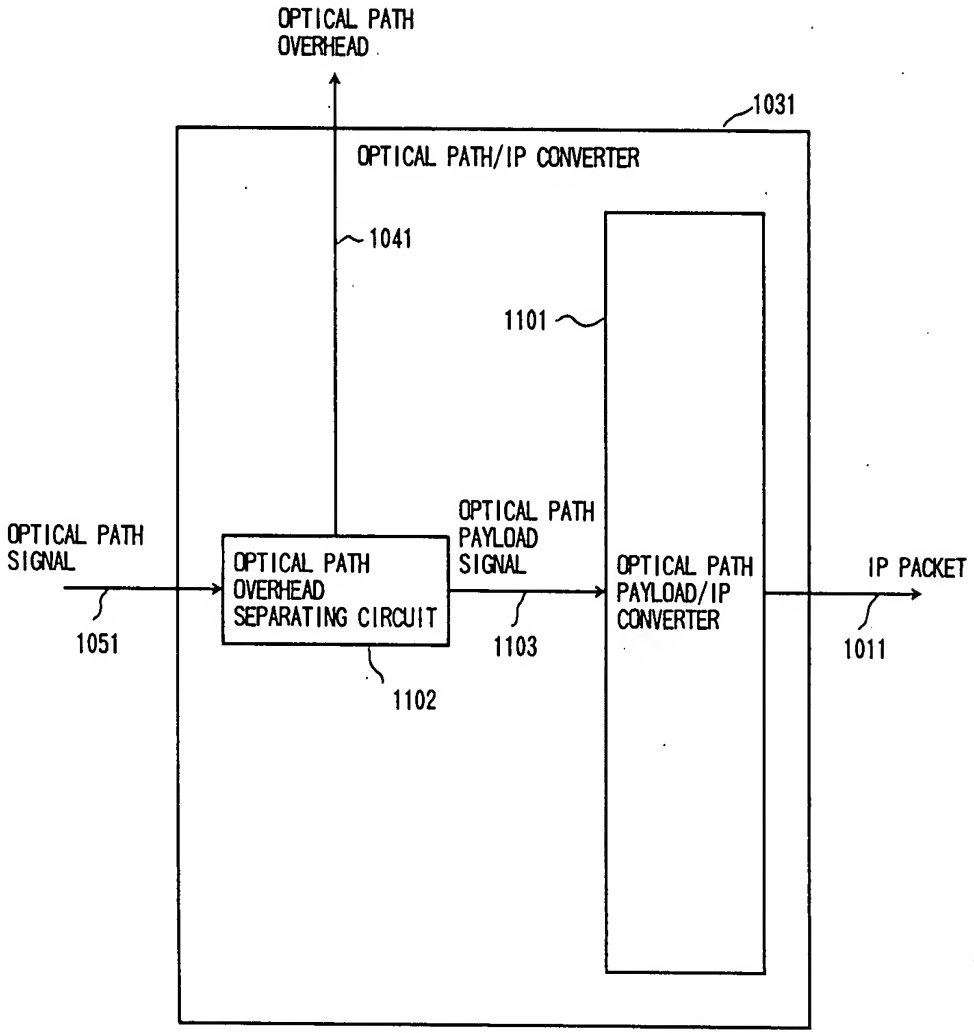
OPTICAL PATH
OVERHEAD
1031
OPTICAL PATH/IP CONVERTER
1041
1101
OPTICAL PATH
SIGNAL
OPTICAL PATH
OVERHEAD
SEPARATING CIRCUIT
OPTICAL PATH
PAYLOAD
SIGNAL
OPTICAL PATH
PAYLOAD/IP
CONVERTER
IP PACKET
1051
1102
1103
1011

FIG. 10

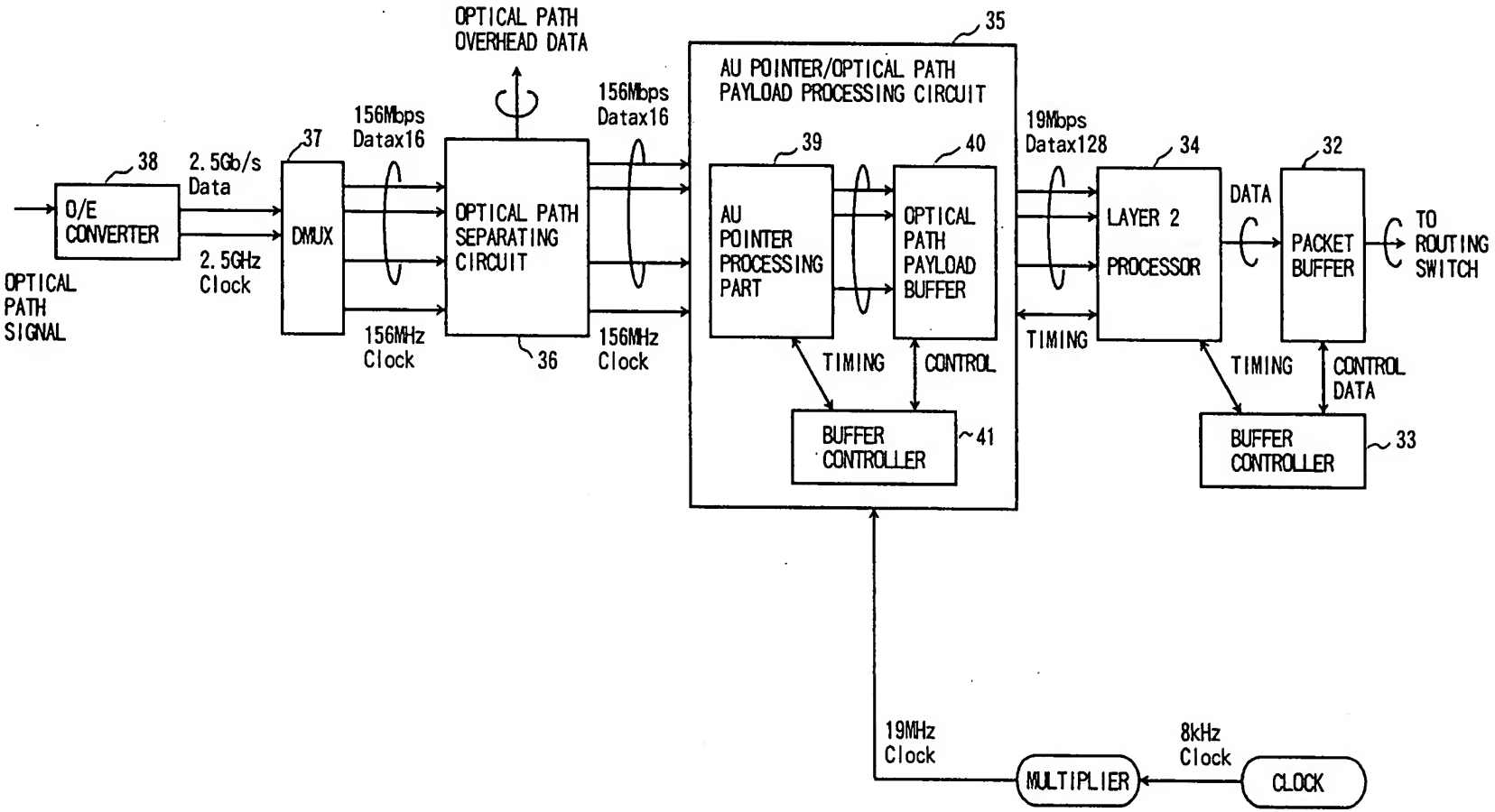
OPTICAL PATH OVERHEAD DATA
35
AU POINTER/OPTICAL PATH PAYLOAD PROCESSING CIRCUIT
156Mbps Datax16
19Mbps Datax128
38
2.5Gb/s Data
37
156Mbps Datax16
39
40
34
32
O/E CONVERTER
DMUX
OPTICAL PATH SEPARATING CIRCUIT
AU POINTER PROCESSING PART
OPTICAL PATH PAYLOAD BUFFER
LAYER 2 PROCESSOR
DATA
PACKET BUFFER
TO ROUTING SWITCH
OPTICAL PATH SIGNAL
2.5GHz Clock
156MHz Clock
36
156MHz Clock
TIMING
CONTROL
TIMING
TIMING
CONTROL DATA
BUFFER CONTROLLER
41
BUFFER CONTROLLER
33
19MHz Clock
8kHz Clock
MULTIPLIER
CLOCK

FIG. 11

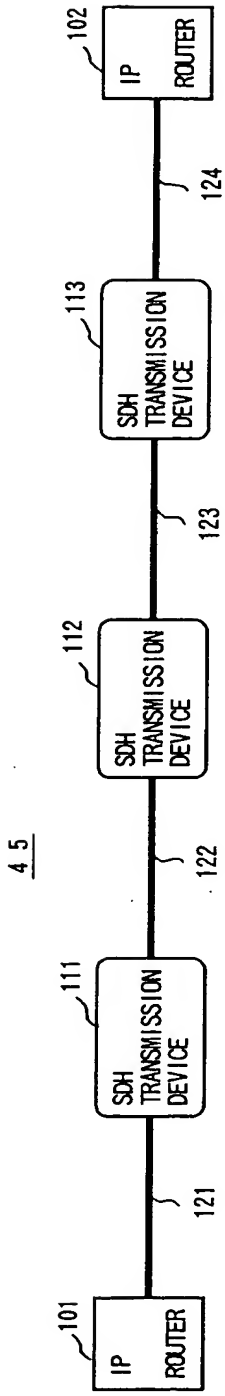
45
101
IP ROUTER
121
111
SDH TRANSMISSION DEVICE
122
112
SDH TRANSMISSION DEVICE
123
113
SDH TRANSMISSION DEVICE
124
102
IP ROUTER

FIG. 12

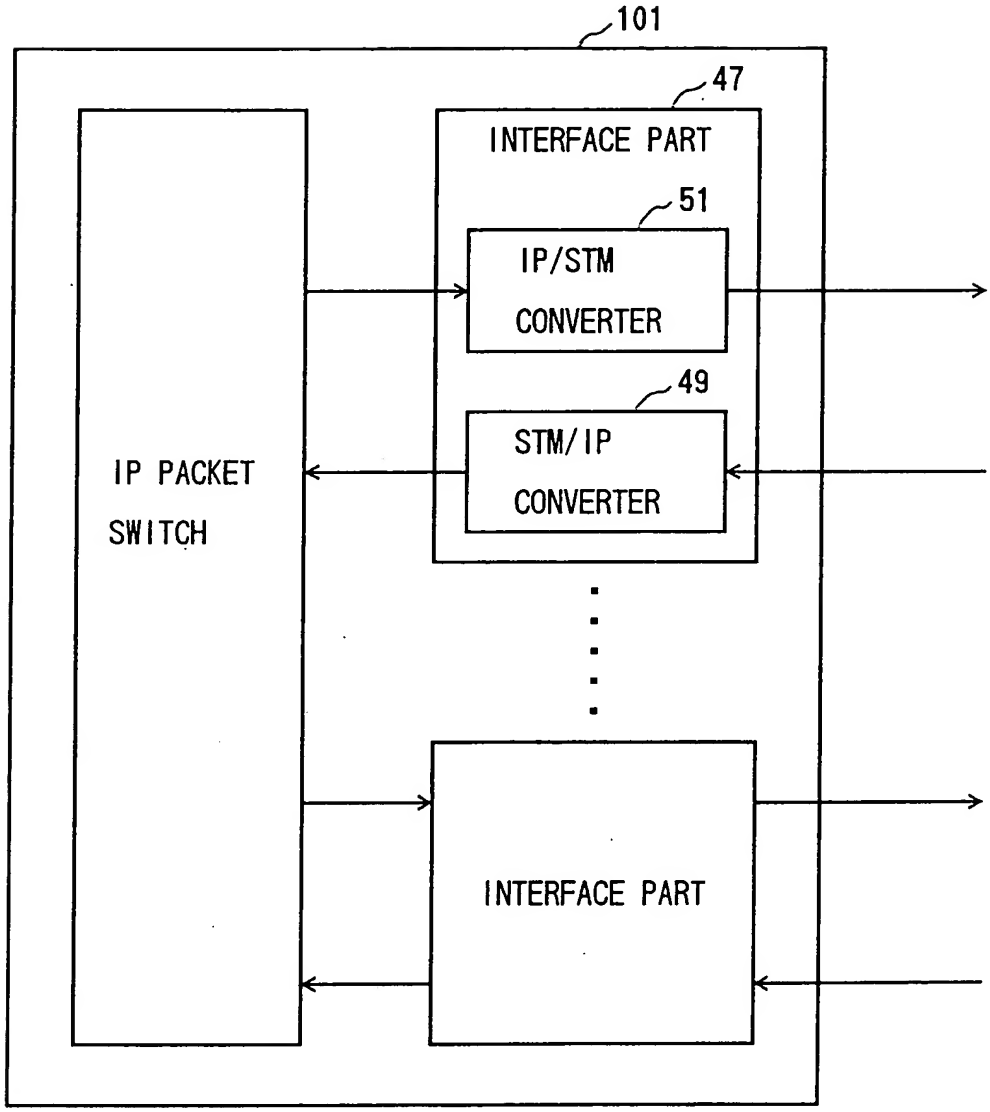
101
47
INTERFACE PART
51
IP/STM
CONVERTER
49
STM/IP
CONVERTER
IP PACKET
SWITCH
INTERFACE PART

FIG. 13

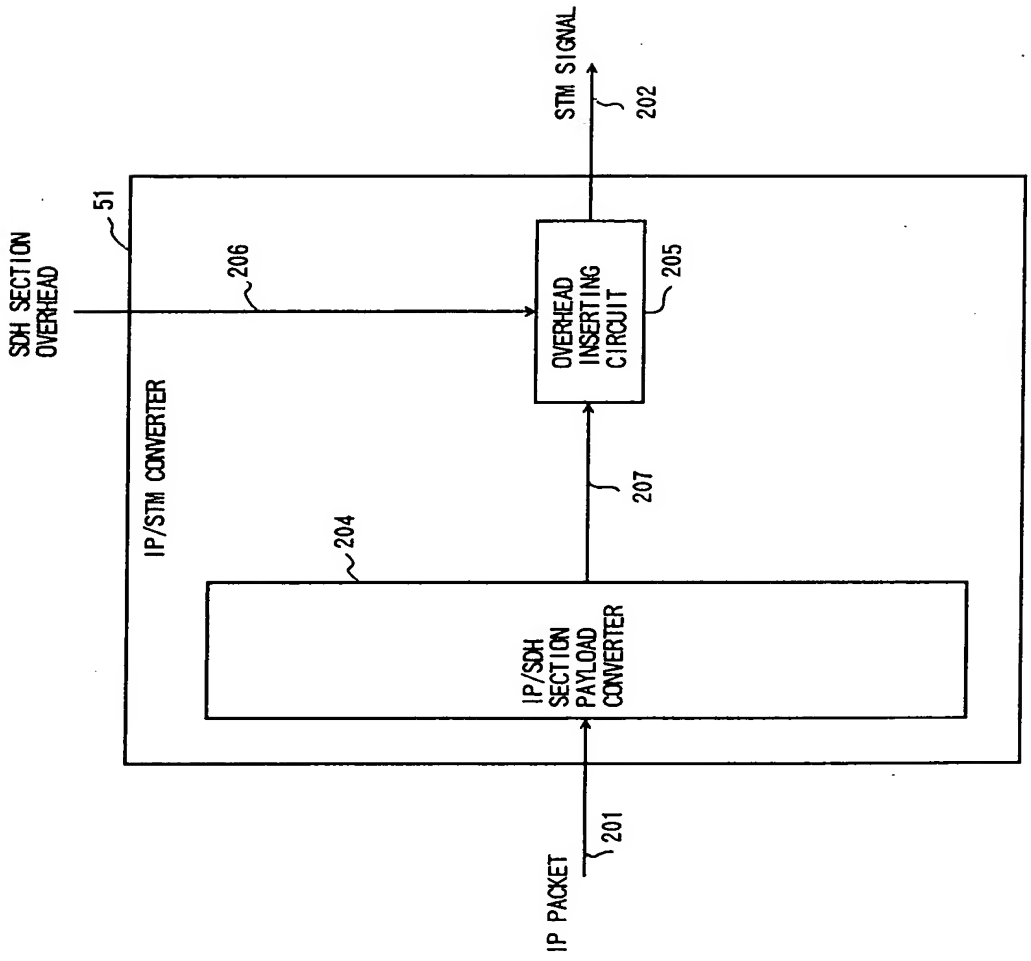
IP PACKET
201
STM SIGNAL
202
SDH SECTION OVERHEAD
51
206
IP/STM CONVERTER
OVERHEAD INSERTING CIRCUIT
205
207
204
IP/SDH SECTION PAYLOAD CONVERTER

FIG. 14

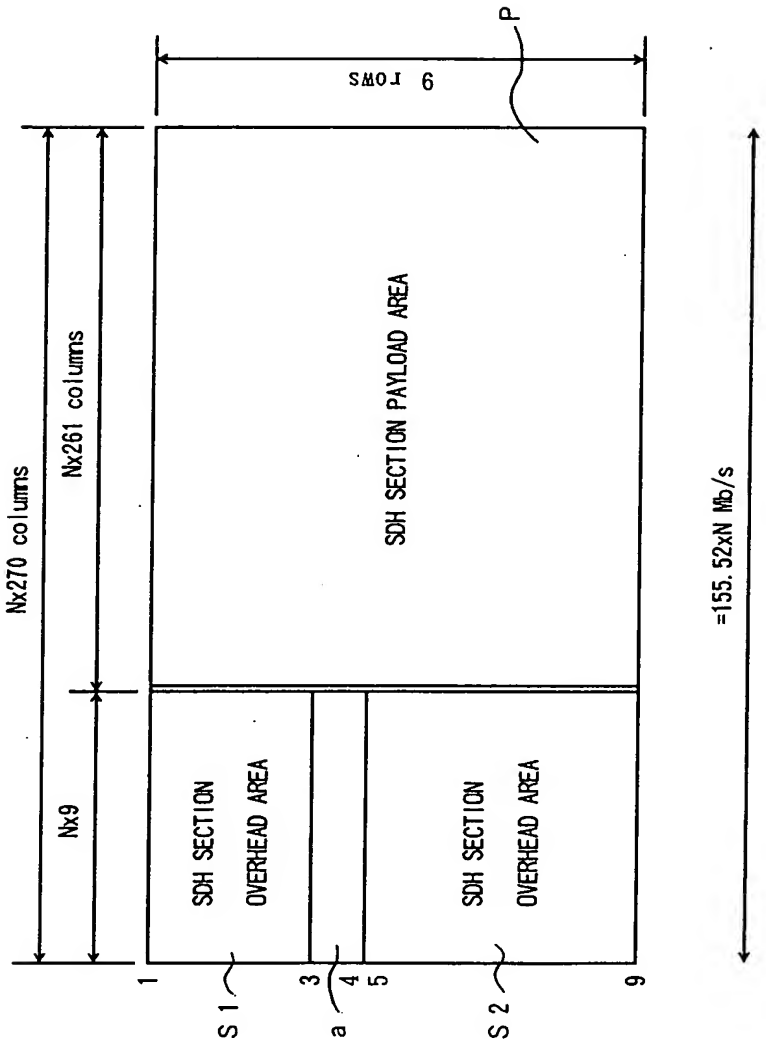
Nx270 columns
Nx261 columns
Nx9
9 rows
P
SDH SECTION PAYLOAD AREA
SDH SECTION OVERHEAD AREA
SDH SECTION OVERHEAD AREA
1
3
4
5
9
S1
a
S2
=155.52xN Mb/s

FIG. 15

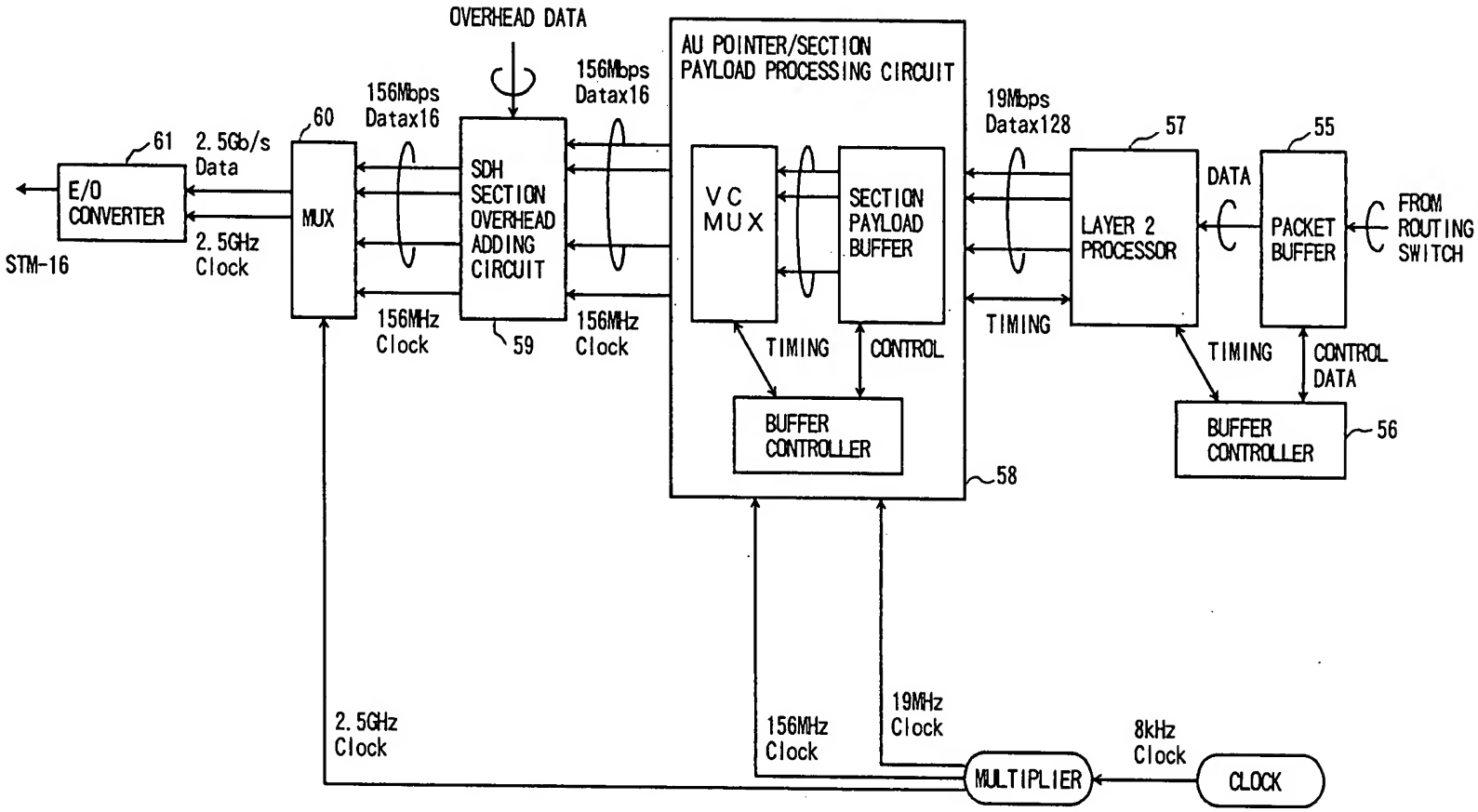
OVERHEAD DATA
AU POINTER/SECTION PAYLOAD PROCESSING CIRCUIT
156Mbps Datax16
156Mbps Datax16
19Mbps Datax128
61
2.5Gb/s Data
60
57
55
E/O CONVERTER
MUX
SDH SECTION OVERHEAD ADDING CIRCUIT
VC MUX
SECTION PAYLOAD BUFFER
LAYER 2 PROCESSOR
DATA
PACKET BUFFER
FROM ROUTING SWITCH
STM-16
2.5GHz Clock
156MHz Clock
59
156MHz Clock
TIMING
CONTROL
TIMING
TIMING
CONTROL DATA
BUFFER CONTROLLER
BUFFER CONTROLLER
56
58
2.5GHz Clock
156MHz Clock
19MHz Clock
8kHz Clock
MULTIPLIER
CLOCK

FIG. 16

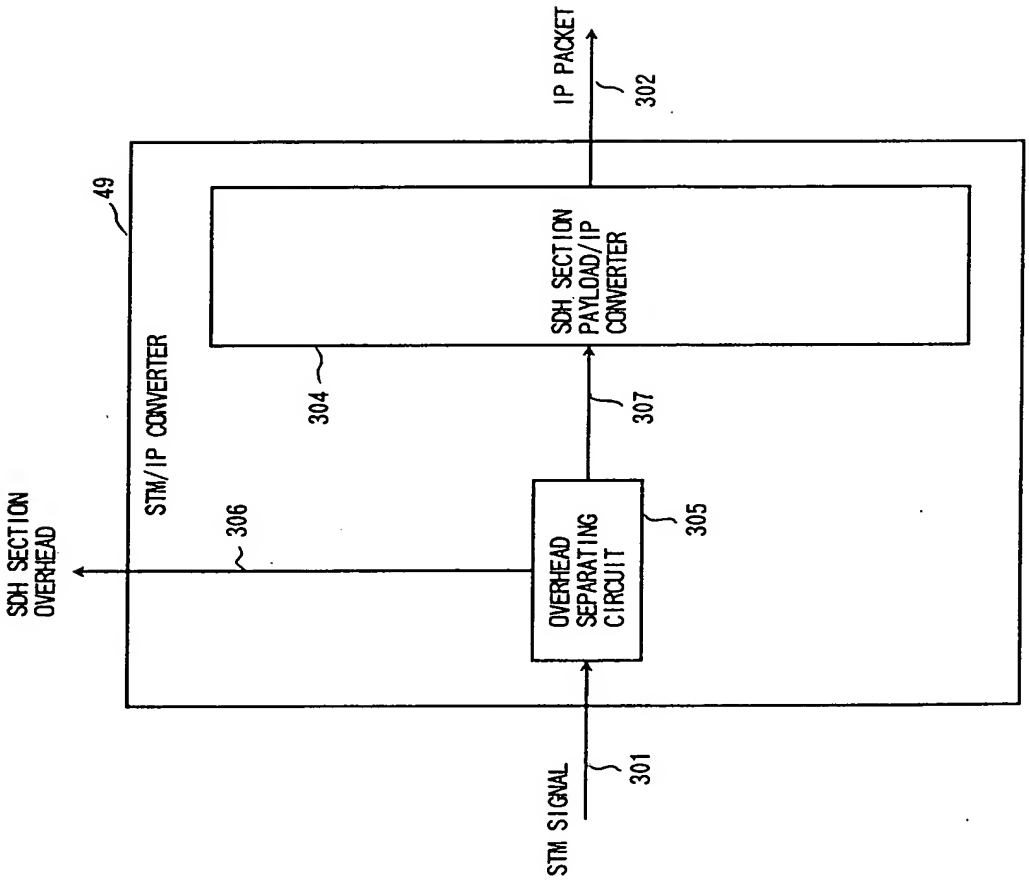
IP PACKET
302
49
STM/IP CONVERTER
SDH SECTION PAYLOAD/IP CONVERTER
304
307
306
OVERHEAD SEPARATING CIRCUIT
305
SDH SECTION OVERHEAD
STM SIGNAL
301

FIG. 17

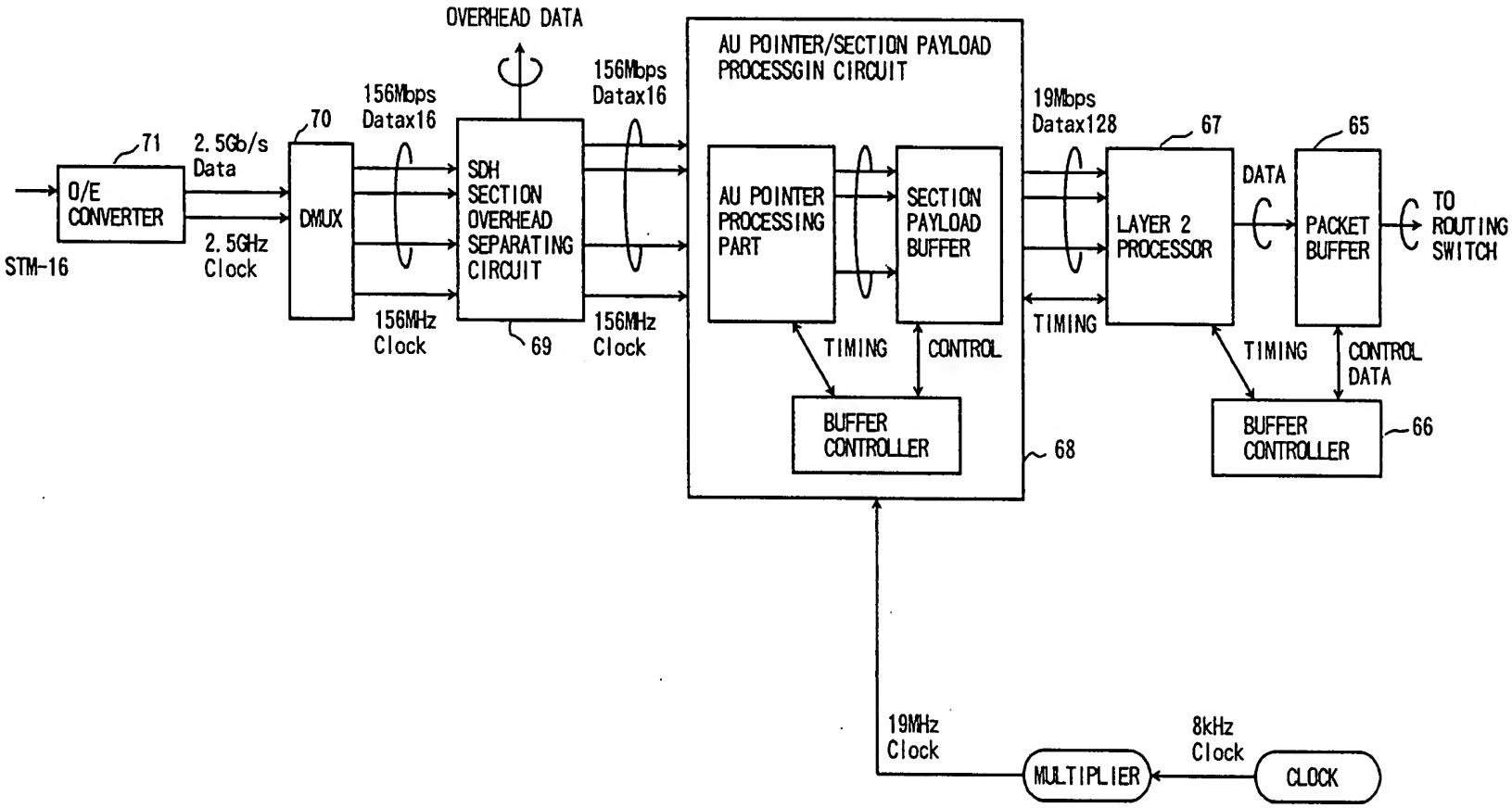
OVERHEAD DATA
AU POINTER/SECTION PAYLOAD PROCESSGIN CIRCUIT
156Mbps Datax16
156Mbps Datax16
19Mbps Datax128
71
70
67
65
2.5Gb/s Data
2.5GHz Clock
O/E CONVERTER
STM-16
DMUX
SDH SECTION OVERHEAD SEPARATING CIRCUIT
69
156MHz Clock
156MHz Clock
AU POINTER PROCESSING PART
SECTION PAYLOAD BUFFER
TIMING
CONTROL
BUFFER CONTROLLER
68
TIMING
LAYER 2 PROCESSOR
DATA
PACKET BUFFER
TO ROUTING SWITCH
TIMING
CONTROL DATA
BUFFER CONTROLLER
66
19MHz Clock
MULTIPLIER
8kHz Clock
CLOCK

FIG. 18
PRIOR ART

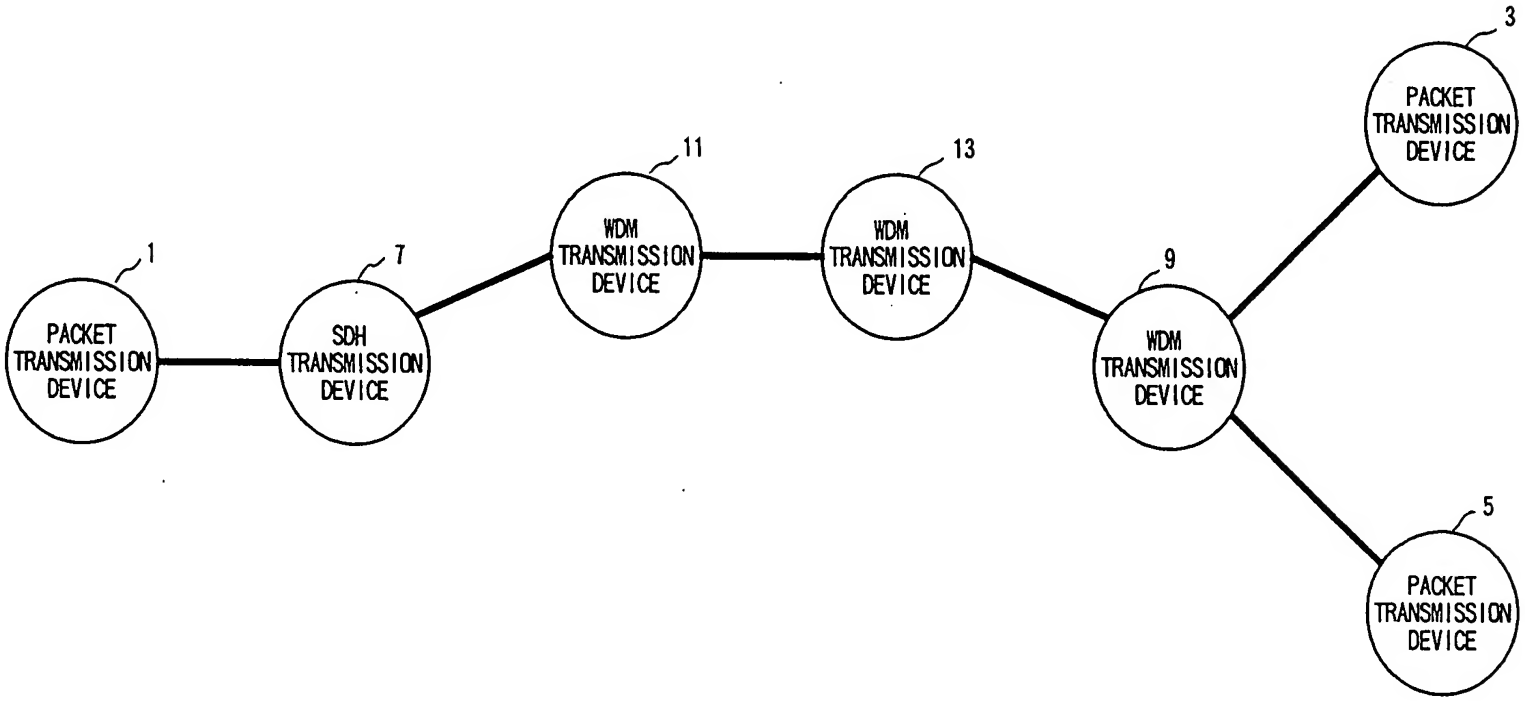

FIG. 19
PRIOR ART

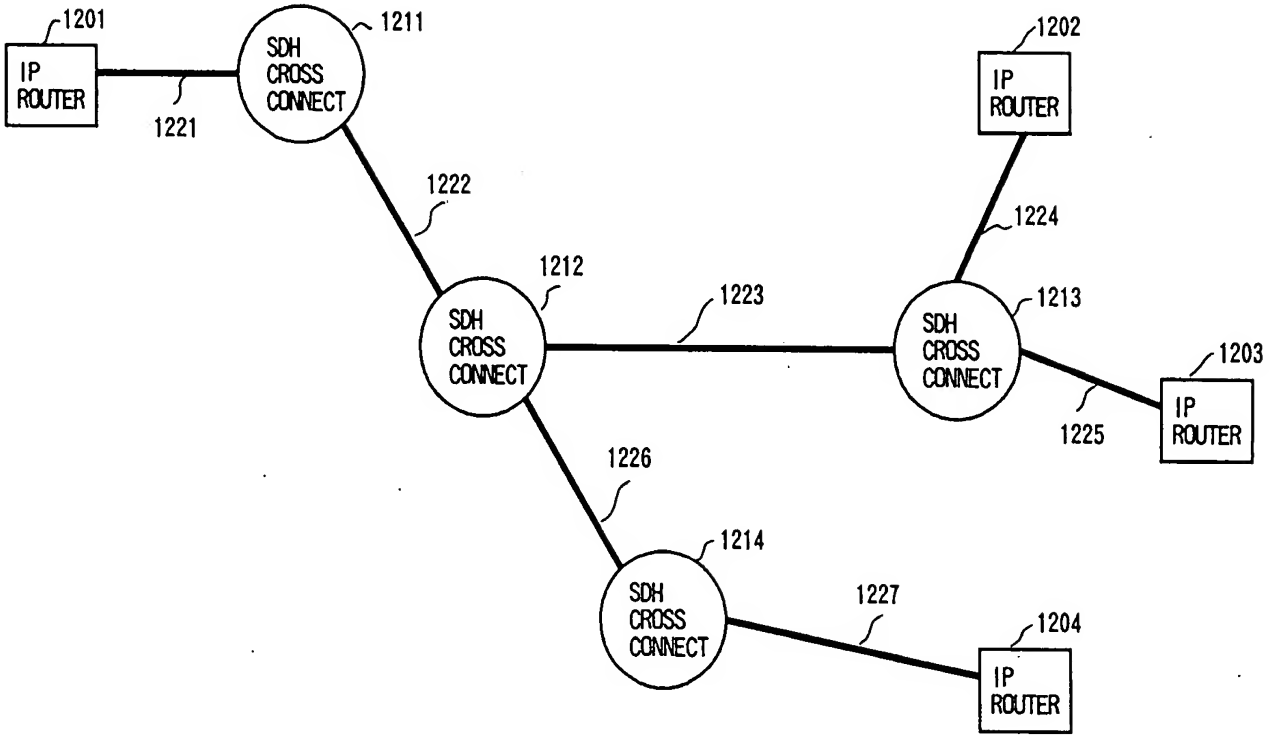

FIG. 20
PRIOR ART

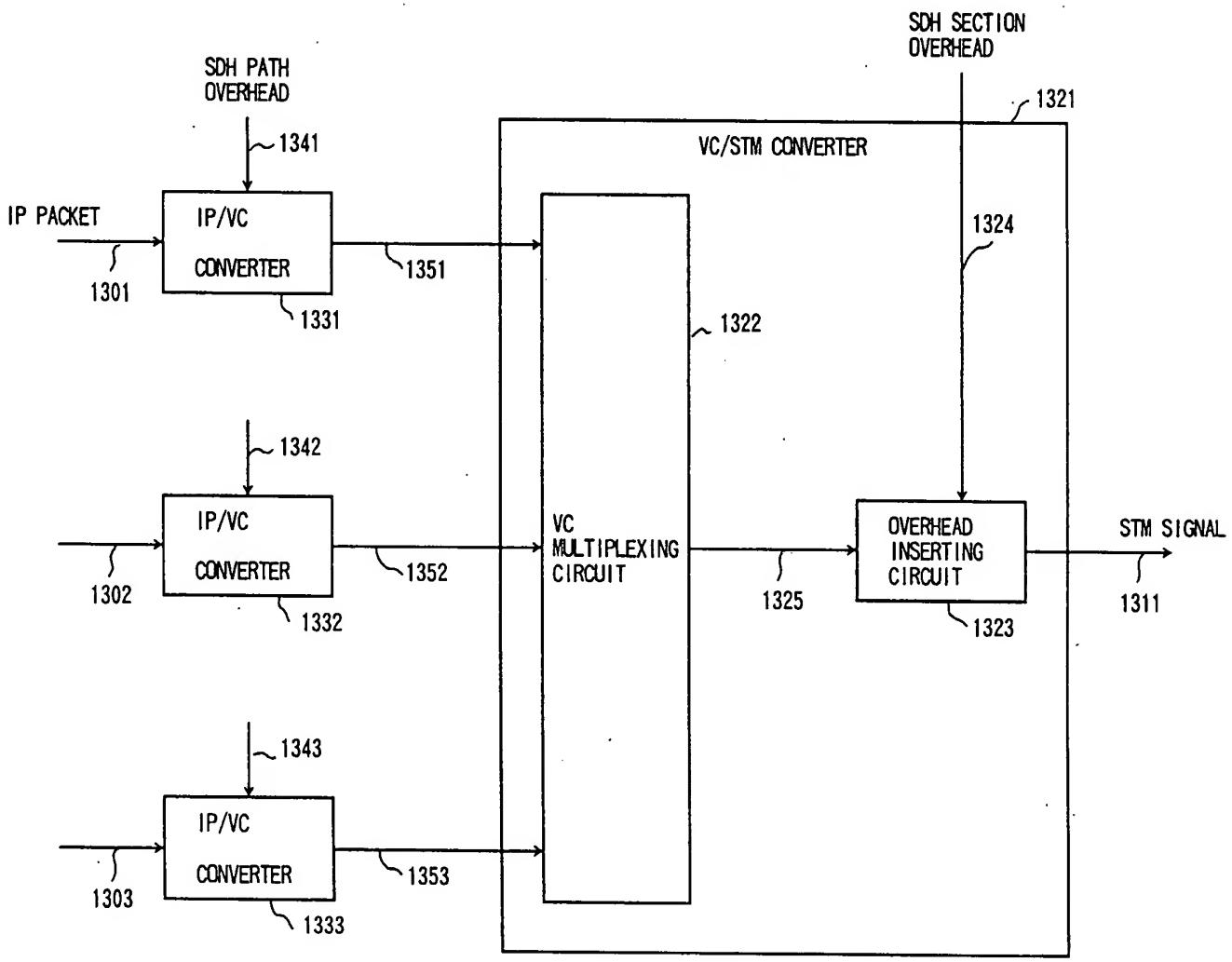
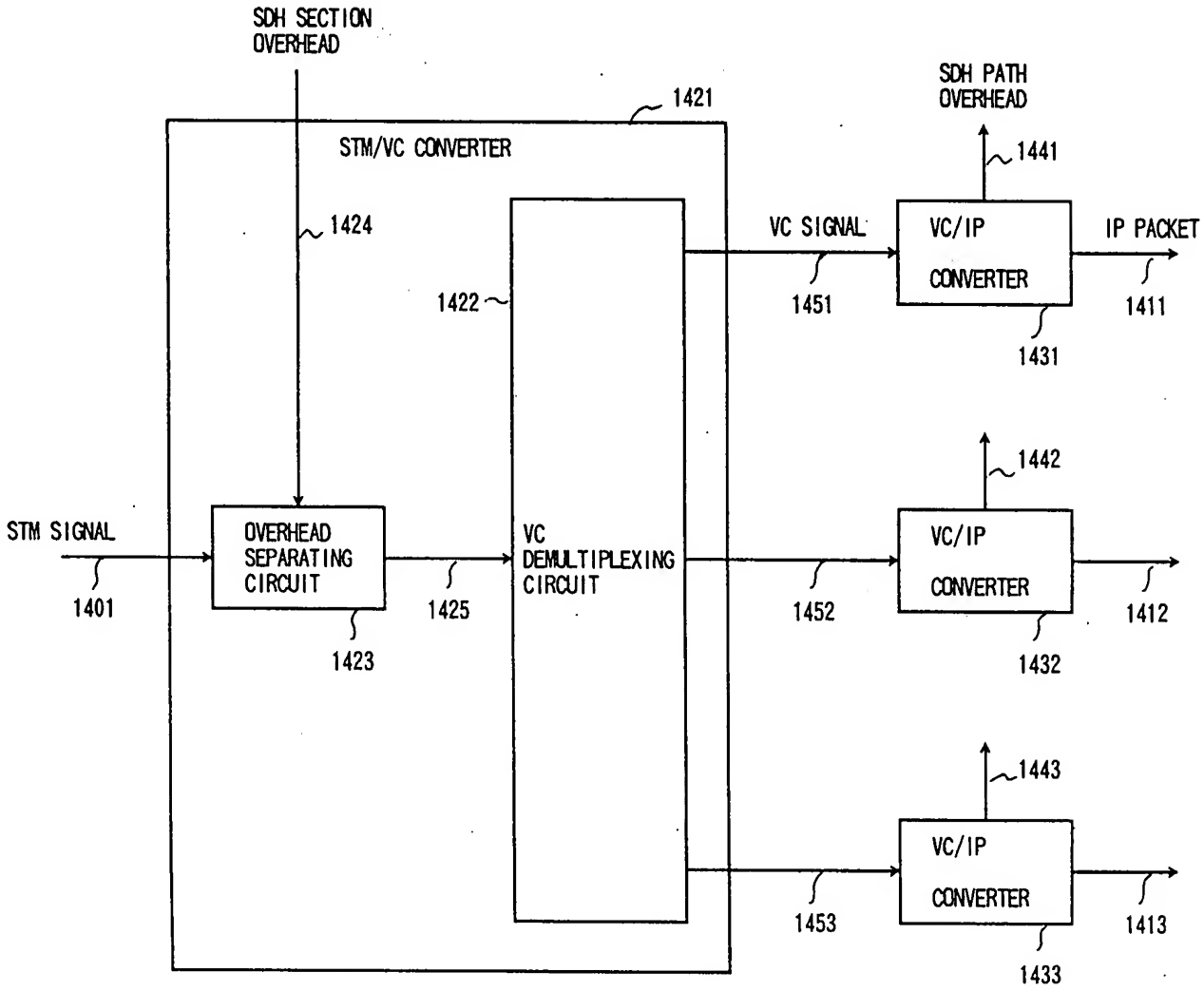
FIG. 21
PRIOR ART